Alternating Input Power Dividing Technique for High Conversion Gain Frequency Doubler

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***Abstract* — This paper presents a new frequency doubler scheme with significant conversion gain improvement. The new design approach utilizes switching operation of FETs. All input power, in this configuration, is directed alternately to each single branch of a pair of parallelly connected FETs corresponding with the polarity of the anti-phase input signal without split of the input power, thereby resulting in enhancing conversion gain. Measurement results demonstrate improvement of 2.87 dB in conversion gain and output power relative to a single-ended structure. For doubling from 5 to 10 GHz the new scheme shows a maximum conversion gain of 11.67 dB.**

I. INTRODUCTION

A balanced configuration has often been used for microwave and millimeter-wave frequency doublers due to high conversion gain and effective suppression of fundamental and odd harmonic frequencies [1-3]. Fundamental and odd harmonic signals are out-of-phase while the desired in phase second harmonics are combined in the balanced configuration. To implement this basic topology, an input power divider such as a 90° hybrid or balun and an output power combiner has typically been incorporated [1-4]. In general, however, by using the input power divider, inevitably the peak voltage of the input sine-wave which is driving a nonlinear device is reduced by a factor of $\sqrt{2}$, weakly driving the device, and thus resulting in reduction of conversion gain.

In this paper, we demonstrate a new frequency doubler configuration by alternately dividing the input power and combining the output power. This design approach, unlike the convention balanced configuration, maintains the peak value of the driving input sine-wave equal to the source signal level, consequently enhancing conversion gain, ideally, up to 3 dB more than that of a single-ended doubler structure.

II. CIRCUIT CONFIGURATION AND OPERATION

The new frequency doubler architecture is based on the fundamental push-pull operation, which uses two FETs biased in class-B. However, in this case the two FETs are not fed using a 3 dB input power divider and an output combiner. Instead a new feeding method is proposed. Fig. 1 shows the simplified circuit diagram of the frequency doubler with two identical branches sharing one output matching circuit designed at the second harmonic.

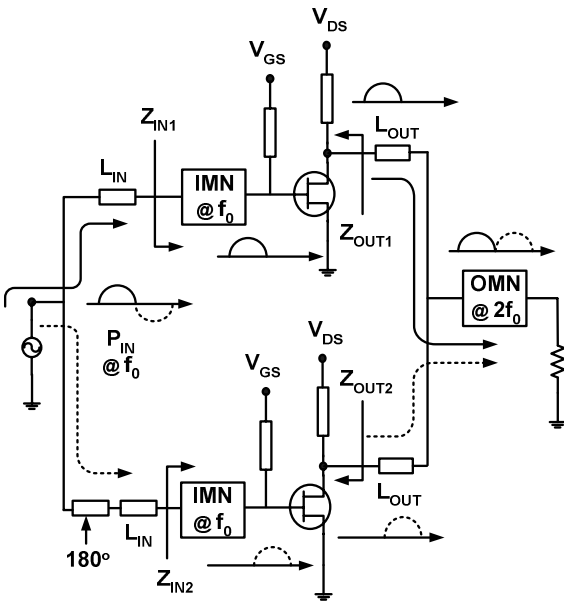

Fig. 1 Circuit diagram of the new frequency doubler (IMN@f_0 and OMN@$2f_0$ are input and output matching networks designed at fundamental and the second harmonic frequencies, respectively)

The input power is fed in anti-phase to the two FETs by adding an 180° phase delay line and the second harmonic output power from each FET is combined together while simultaneously nulling the out-of-phase fundamental frequency signals.

When FETs are in the pinch-off operation region, the input and output impedances are nearly purely reactive [5-6]. Therefore, as shown in Fig.1, the microstrip transmission line, L_{IN} causes the impedance looking into the lower branch driven into pinch-off, Z_{IN2}, to be transformed to high impedance value, ideally open, during positive half-cycle of the input signal. Similarly, when the lower branch is conducting during negative half-cycle, Z_{IN1} is transformed to high impedance value. Thus, the input sine-wave signal, in half-rectified waveform, is

fed to FETs on alternating half-wave cycles without reduction of its peak value by a factor of $\sqrt{2}$. In a similar fashion at the input side, L_{OUT} at an output matching side serves the same function as L_{IN}, transforming Z_{OUT1} or Z_{OUT2} to a high impedance value corresponding with the polarity of the input signal. As a result, at the positive half-wave cycles, power is diverted to only the upper FET and signal passes through the upper branch. The negative cycles, dashed line in Fig.1, are fed to the other FET through the lower branch.

III. Design and Measurement Results

The circuit operation described in the previous section was applied in designing a 5 to 10 GHz frequency doubler. The packaged 280μm-wide NEC 76038 GaAs FET nonlinear model was utilized in the Agilent ADS harmonic balance simulator. The design was based on an optimum output impedance for maximum output power at the desired second harmonic extracted from the load-pull simulation.

A single-ended frequency doubler was designed based on the output impedance. In this design step, the L_{OUT} was added at the output side as a part of an output matching network in order to transform Z_{OUT1} or Z_{OUT2} to a high impedance value when the corresponding FET is driven beyond pinch-off. Besides the optimization of the output impedance, a second-harmonic frequency reflector was added in the input matching side to improve conversion gain performance of the designed doubler scheme [7-8]. A resonator designed at the 5 GHz fundamental frequency was utilized for the reflector and placed at the input matching side in parallel with signal path. Thus, it generates purely reactive impedance at the 10 GHz second harmonic frequency. In practice, the designed reflector was implemented by means of the stepped impedance resonator [9].

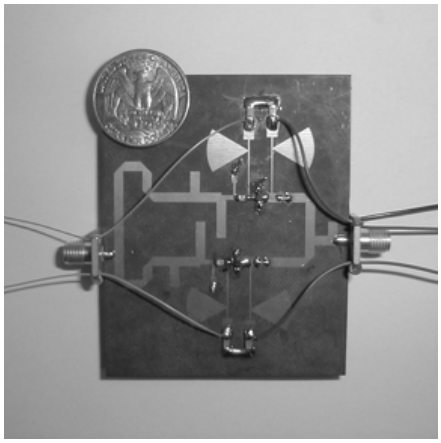

Fig. 2 Photograph of the new double-branch frequency doubler

Two of these structures were combined by adding an extra transmission line, L_{IN}, serving the same purpose at the input side as L_{OUT} at the output and a 180° phase delay line providing a differential excitation. The designed single-ended and double-branch frequency doublers were fabricated on Duroid substrate with εr=2.33 and thickness of 31 mils. The photograph of the fabricated new double-branch frequency doubler is shown in Fig. 2.

For testing large-signal performance, the bias voltages were set to V_{DS} of 3 V and V_{GS} of -0.8 V, pinch-off operation region. First, a single-ended structure, consisting of one branch of the double-branch structure including the output matching circuit, was tested with a 5 GHz input frequency. Fig. 3 shows the measured output power at 10 GHz and the conversion gain with respect to the input power. An output power of 7.3 dBm and a conversion gain of 6.3 dB at an input power of 1 dBm were obtained.

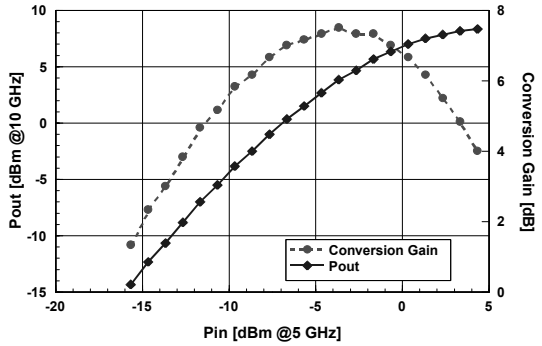

Fig. 3 Measured output power (P_{out}) and conversion gain for the single-ended frequency doubler

The same bias voltages were applied for testing the new double-branch structure. The measured second harmonic output power and conversion gain is shown in Fig, 4 as a function of the input power. At 1 dBm input power level, an output power of 10.17 dBm and a conversion gain of 9.17 dB were measured.

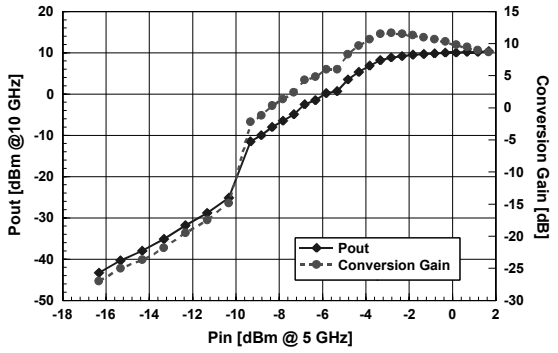

Fig. 4 Measured output power (P_{out}) and conversion gain for the double-branch frequency doubler

By alternately selecting each branch in the double-branch configuration depending on the polarity of the

input signal and without reducing peak of the input signal, 2.87 dB improvement in conversion gain and output power was achieved compared to the measurement data of the single-ended structure. Due to finite impedance value, in practice, it causes a loading effect from one branch to the other so that the improvement is smaller than ideal 3 dB.

As clearly shown in Fig. 4, abrupt increase of output power occurs when the input power level is about -10 dBm. This phenomenon can be explained by noticing that when the input power is not sufficient to drive each FET in the proposed switching mode operation the input power is divided between both branches unequally instead of one branch at a time so that the second harmonic output power is reduced due to the differential phase difference. However, once the input power level reaches a sufficient power level to drive each FET alternately, it starts to operate properly by selecting a single branch corresponding with the input signal cycle.

In this circuit configuration, due to the 180^{o} delay line at the lower branch, differential excitation occurs for the 5 GHz fundamental input signal. By combining two branches at the output matching side, the out-of-phase fundamental frequency signal can effectively be suppressed. The measured suppression characteristics for the fundamental frequency of 5 GHz and 15 GHz third harmonic frequencies with respect to the input power range from -10 to 2 dBm are shown in Fig. 5.

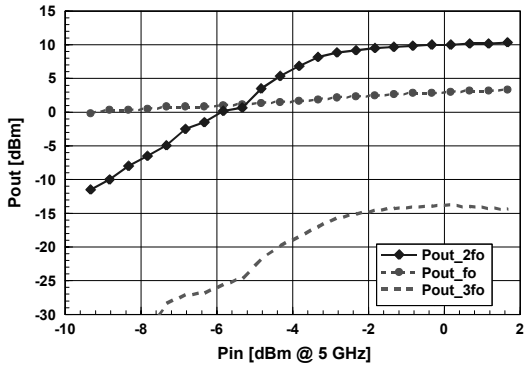

Fig. 5 Measured suppression characteristics of the double-branch frequency doubler

Note that the shown suppression characteristics are measured once the doubler was operating in the desirable operation. Relative to the 10 GHz frequency signal power, the suppression was -7.16 dBc for 5 GHz and -30 dBc for the 15 GHz. The measured suppression characteristic results are not as low as simulation results which show -50 dBc for the fundamental frequency using a FET nonlinear model in ADS. This discrepancy may be caused by imperfections in the implementation of hybrid microwave circuits and inaccurate transistor model, especially, in the pinch-off region. Suppression may be enhanced by accurately controlling phase delay at the fundamental frequency and improving the transistor nonlinear model to be biased to class-B.

IV. CONCLUSION

A new frequency doubler configuration has been demonstrated. In this scheme, conversion gain and output power performance can be improved ideally up to 3 dB more than those of an identical single-ended structure by alternately dividing input power and combining output power.

For the new double-branch configuration, a 9.17 dB conversion gain and 10.17 dBm output power were obtained at designed 10 GHz. When compared to the measured performance of a single-ended doubler, improvement of 2.87 dB in conversion gain an output power was achieved. An 11.67 dB maximum conversion gain and 10.34 dBm saturated output power were measured from the new doubler configuration.

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